TLA5200 Series Logic Analyzer
Product Specifications & Performance Verification

Technical Reference

077-2502-01

Tektronix

TLA5200 Series Logic Analyzer
Product Specifications & Performance Verification

Technical Reference

This document applies to TLA System Software Version 5.1SP1 and above

Warning

These servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

www.tektronix.com

077-2502-01

Tektronix

Contacting Tektronix

Tektronix, Inc.
14200 SW Karl Braun Drive
P.O. Box 500
Beaverton, OR 97077
USA

For product information, sales, service, and technical support:

- In North America, call 1-800-833-9200.
- Worldwide, visit www.tektronix.com to find contacts in your area.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of a larger system. Read the safety sections of the other component manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

The inputs are not rated for connection to mains or Category II, III, or IV circuits.

Power Disconnect. The power cord disconnects the product from the power source. Do not block the power cord; it must remain accessible to the user at all times.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Do Not Operate With Suspected Failures. If you suspect that there is damage to this product, have it inspected by qualified service personnel.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Terms in this Manual

These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Symbols and Terms on the Product

These terms may appear on the product:

- DANGER indicates an injury hazard immediately accessible as you read the marking.
- WARNING indicates an injury hazard not immediately accessible as you read the marking.
- CAUTION indicates a hazard to property including the product.

The following symbol(s) may appear on the product:

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface

This document lists the characteristics and specifications of the TLA5200 and TLA5200B series logic analyzers. It also includes the performance verification procedures. All references to TLA5200 also apply to TLA5200B, unless otherwise noted. Microprocessor-related products and individual logic analyzer probes have their own documentation for characteristics and specifications.

To prevent personal injury or damage consider the following requirements before attempting service:

- The procedures in this manual should be performed only by qualified service personnel.
- Read the General Safety Summary and Service Safety Summary found at the beginning of this manual.

Be sure to follow all warnings, cautions, and notes in this manual.

Related Documentation

The following table lists related documentation available for your logic analyzer. The documentation is available on the TLA Documentation CD included with your logic analyzer, and on the Tektronix Web site (www.Tektronix.com).

To obtain documentation not specified in the table, contact your local Tektronix representative.

Table i: Related Documentation

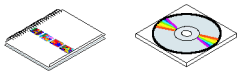
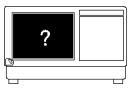
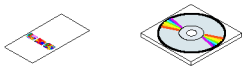
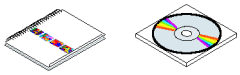
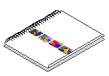
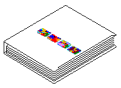
Item	Purpose	Location
TLA Quick Start User Manual	Basic operational overview	
Online Help	In depth operation and UI help	
Installation Quick Reference Cards	Basic installation information	
Installation Manuals	Detailed first-time installation information	
XYZs of Logic Analyzers	Introduction to logic analyzer basics	 www.Tektronix.com
TLA Product Specifications	Specifications for other TLA products	

Table i: Related Documentation (cont.)

Item	Purpose	Location
TPI.NET Documentation	Detailed information for controlling the logic analyzer using .NET	
Field upgrade kits	Upgrade information for your logic analyzer product	 
Optional Service Manuals	Self-service documentation for modules and mainframes	 
TLA Application Software Release Notes	Software description, compatibility, impact of changes, contact information, installation, upgrade, and operational notes, and known issues.	 Go to Start→All Programs→Tektronix logic Analyzer→TLA Release Notes

Specifications

The following tables list the specifications for the TLA5200B and TLA5200 series logic analyzers. All references to TLA5200 also apply to TLA5200B, unless otherwise noted. All specifications are guaranteed unless noted *Typical*. Typical characteristics describe typical or average performance and provide useful reference information.

Specifications that are marked with the ✓ symbol are checked directly (or indirectly) in the *Performance Verification* chapter of this document.

The performance limits in this specification are valid with these conditions:

- The instrument must be in an environment with temperature, altitude, humidity, and vibration within the operating limits described in these specifications.
- The instrument must have had a warm-up period of at least 30 minutes.
- The instrument must have been calibrated/adjusted at an ambient temperature between +20 °C and +30 °C.

For optimum performance using an external oscilloscope, please consult the documentation for any external oscilloscopes used with your Tektronix logic analyzer to determine the warm-up period and signal-path compensation requirements.

Table 1: Atmospheric characteristics

Characteristic	Description
Temperature	*Operating (no media in CD or DVD drive)*
	+5 °C to +50 °C, 15 °C/hr maximum gradient, noncondensing (derated 1 °C per 305 m (1000 ft) above 1524 m (5000 ft) altitude)
	Nonoperating (no media in drive)
	-20 °C to +60 °C, 15 °C/hr maximum gradient, noncondensing
Relative humidity	*Operating (no media in drive)*
	20% to 80% relative humidity, noncondensing. Maximum wet bulb temperature: +29 °C (derates relative humidity to approximately 22% at +50 °C).
	Nonoperating (no media in drive)
	8% to 80% relative humidity, noncondensing. Maximum wet bulb temperature: +29 °C (derates relative humidity to approximately 22% at +50 °C).
Altitude	*Operating*
	To 3000 m (9843 ft), (derated 1 °C per 305 m (1000 ft) above 1524 m (5000 ft) altitude.
	Nonoperating
	12,190 m (40,000 ft)

Table 2: TLA5200 input parameters with probes

Characteristic		Description	
✓ Threshold Accuracy		±100 mV	
Threshold range and step size		Settable from +4.5 V to -2 V in 5 mV steps	
Threshold channel selection		16 threshold groups assigned to channels. P6410, P6417, P6418, and P6419 probes have two threshold settings, one for the clock/qualifier channel and one for the data channels. P6434 probes have four threshold settings, one for each of the clock/qualifier channels and two for the data channels (one per 16 data channels).	
✓ Channel-to-channel skew		≤ ±150 ps maximum	
Channel-to-channel skew *(Typical)*		≤ ±75 ps	
Sample uncertainty		*Asynchronous*	*Synchronous*
		Sample period	125 ps
Input voltage range		–2.5 to +5 V	
Probe input resistance *(Typical)*		20 kΩ	
Probe input capacitance *(Typical)*	P6410, P6417, P6434	2 pF	
	P6418	1.4 pF data channels	
		2 pF CLK/Qual channels	
	P6419	< 0.7 pF	
Minimum slew rate *(Typical)*		0.2 V/ns	
Maximum operating signal		6.0 V_{p-p}	
Probe overdrive	P6410, P6417, P6418, P6419	±250 mV or ±25% of signal swing minimum required beyond threshold, whichever is greater	
	P6434	±300 mV or ±25% of signal swing minimum required beyond threshold, whichever is greater	
		±4 V maximum beyond threshold	
Maximum nondestructive input signal to probe		±15 V	
Minimum input pulse width signal (single channel) *(Typical)*		1.5 ns (P6434)	
		1.25 ns (P6410, P6417, P6418, P6419)	
Delay time from probe tip to module input probe connector *(Typical)*		7.33 ns ±100ps	

Table 3: TLA5200 timing latencies

Characteristic		Description
System Trigger and External Signal Input Latencies [1] *(Typical)*	External System Trigger Input to LA Probe Tip [2]	–656 ns
	External Signal Input to LA Probe Tip via Signal 3, 4	–656 ns + Clk [3]
	External Signal Input to LA Probe Tip via Signal 1, 2 [4]	–656 ns + Clk [3]

Table 3: TLA5200 timing latencies (cont.)

Characteristic			Description
System Trigger and External Signal Output Latencies *(Typical)*	LA Probe Tip to External System Trigger Out [5] [6]		778 ns + SMPL
	LA Probe Tip to External Signal Out via Signal 3, 4 [5] [6]	OR function	772 ns + SMPL
		AND function	772 ns + SMPL
	LA Probe Tip to External Signal Out via Signal 1, 2 [4] [5] [6]	normal function	772 ns + SMPL
		inverted logic on backplane	774 ns + SMPL

1 All system trigger and external signal input latencies are measured from a falling-edge transition (active true low) with signals measured in the wired-OR configuration.

2 In the Waveform window, triggers are always marked immediately except when delayed to the first sample. In the Listing window, triggers are always marked on the next sample period following their occurrence.

3 CLK represents the time to the next master clock at the destination. In Normal clocking, this represents the delta time to the next sample clock. In External clocking, this represents the time to the next master clock generated by the setup of the clocking state machine and the supplied SUT clocks and qualification date.

4 Signals 1 and 2 (ECLTRG 0, 1) are limited to a "broadcast" mode of operation, where only one source is allowed to drive the signal node at any one time. That single source can be used to drive any combination of destinations.

5 SMPL represents the time from the event to the next valid data sample at the probe tip input. In the Normal Internal clock mode, this represents the delta time to the next sample clock. In the MagniVu Internal clock mode, this represents 125 ps. In the External clock mode, this represents the time to the next master clock generated by the setup of the clocking state machine, the SUT-supplied clocks, and the qualification data.

6 All signal output latencies are validated to the rising edge of an active (true) high output.

Table 4: TLA5200 external signal interface

Characteristic		Description	
System trigger input		TTL compatible input via rear panel mounted BNC connectors	
	Input destination	System trigger	
	Input levels	TTL compatible input	
	V_{IH}	≥ 2.0 V	
	V_{IL}	≤ 0.8 V	
	Input mode	Falling edge sensitive, latched (active low)	
	Minimum pulse width	12 ns	
	Active period	Accepts system triggers during valid acquisition periods via real-time gating, resets system trigger input latch between valid acquisition periods.	
	Maximum input voltage	0 to +5 V peak	
External signal input		TTL compatible input via rear panel mounted BNC connectors	
	Input destination	Signal 1, 2, 3, 4	
	Input levels	TTL compatible input	
	V_{IH}	≥ 2.0 V	
	V_{IL}	≤ 0.8 V	
	Input mode	Active (true) low, level sensitive	
	Input bandwidth [1]	*Signal 1, 2*	*Signal 3, 4*
		50 MHz square wave minimum	10 MHz square wave minimum
	Active period	Accepts signals during valid acquisition periods via real-time gating.	
	Maximum input voltage	0 to +5 V peak	

Table 4: TLA5200 external signal interface (cont.)

Characteristic		Description	
System trigger output		TTL compatible output via rear panel mounted BNC connectors	
	Source selection	System trigger	
	Source mode	Active (true) low, falling edge latched	
	Active period	Outputs system trigger state during valid acquisition period, resets system trigger output to false state between valid acquisitions	
	Output levels	50 Ω back terminated TTL-compatible output	
	V_{OH}	≥4 V into open circuit	
		≥ 2 V into 50 Ω to ground	
	V_{OL}	≤ 0.7 V sinking 10 mA	
	Output protection	Short-circuit protected (to ground)	
External signal output		TTL compatible outputs via rear panel mounted BNC connectors	
	Source selection	Signal 1, 2, 3, 4, or 10 MHz clock	
	Output modes level sensitive	User definable active (true) low or active (true) high	
	Output levels	50 Ω back terminated TTL output	
	V_{OH}	≥4 V into open circuit	
		≥2 V into 50 Ω to ground	
	V_{OL}	≤ 0.7 V sinking 10 mA	
	Output bandwidth [2]	*Signal 1, 2*	*Signal 3, 4*
		50 MHz square wave minimum	10 MHz square wave minimum
	Active period	Outputs signals during valid acquisition periods, resets signals to false state between valid acquisitions	
		Outputs 10 MHz clock continuously	
	Output protection	Short-circuit protected (to ground)	

1 The input bandwidth specification only applies to signals to the External Signal input; it does not apply to signals applied to the External Signal input and sent back to the External Signal output.

2 The output bandwidth specification only applies to signals to the External Signal output; it does not apply to signals applied to the External Signal output and sent back to the External Signal input.

Table 5: TLA5200 channel width and depth

Characteristic	Description	
Number of channels	*Product*	*Channels*
	TLA5201	32 data and 2 clock
	TLA5202	64 data and 4 clock
	TLA5203	96 data, 4 clock, and 2 qualifier
	TLA5204	128 data, 4 clock, and 4 qualifier
Acquisition memory depth	*Product*	*Memory depth*
	TLA520XB	2 M or optionally 8 M or 32 M samples [1]
	TLA520X	512 K or optionally 2 or 8 M samples [1]

[1] PowerFlex options

Table 6: Reference clock (CLK10)

Characteristic	Description
✓ Clock accuracy	10 MHz ±100 ppm

Table 7: TLA5200 clocking

Characteristic	Description	
Asynchronous clocking		
✓ Internal sampling period [1]	500 ps to 50 ms in a 1-2-5 sequence. Storage control can be used to only store data when it has changed (transitional storage)	
	2 ns minimum for all channels	
	1 ns minimum for half channels (using 2:1 demultiplex mode)	
	0.5 ns minimum for quarter channels (using 4:1 demultiplex mode)	
✓ Minimum recognizable word [2] (across all channels)	Channel-to-channel skew + sample uncertainty	
	Example: for a 2 ns sample period and a P6419, or P6434 Probe = 400 ps + 2 ns = 2.4 ns	
Synchronous clocking		
Number of master clock channels [3]	*Product*	*Clock Channels*
	TLA5201	2
	TLA5202	4
	TLA5203	4
	TLA5204	4
Number of qualifier channels [4]	*Product*	*Qualifier Channels*
	TLA5201	0
	TLA5202	0
	TLA5203	2
	TLA5204	4
✓ Setup and hold window size	1 ns maximum, any clock to any single data or qualifier channel	
Setup and hold window size *(Typical)*	1.5 ns, all channels	

Table 7: TLA5200 clocking (cont.)

Characteristic	Description	
Setup and hold window range	For each channel, the setup and hold window can be moved from +8.0 ns (Ts) to -8.0 ns (Ts) in 0.125 ns steps. The hold time follows the setup time by the setup and hold window size.	
✓ Maximum synchronous clock rate	235 MHz in full speed mode (4.25 ns minimum between active clock edges)	
2X Demux clocking		
TLA5203, TLA5204	Any individual channel may be demultiplexed with its partner channel. Channels demultiplex as follows:	
	A3(7:0) to/from	D3(7:0)
	A2(7:0) to/from	D2(7:0)
	A1(7:0) to/from	D1(7:0)
	A0(7:0) to/from	D0(7:0)
	C3(7:0) to/from	C1(7:0)
	C2(7:0) to/from	C0(7:0)
	E3(7:0) to/from	E1(7:0) (TLA5204 only)
	E2(7:0) to/from	E0(7:0) (TLA5204 only)
	CK3 to/from	Q2 (TLA5204 only)
	CK2 to/from	Q3 (TLA5204 only)
	CK1 to/from	Q0
	CK0 to/from	Q1
TLA5201, TLA5202	Any individual channel may be demultiplexed with its partner channel. Channels demultiplex as follows:	
	A3(7:0) to/from	C3(7:0)
	A2(7:0) to/from	C2(7:0)
	A1(7:0) to/from	D1(7:0) (TLA5202 only)
	A0(7:0) to/from	D0(7:0)(TLA5202 only)
Time between Demultiplex clock edges *(Typical)*	Same limitations as normal synchronous acquisition	
4X Demux clocking		
TLA5203, TLA5204	Unlike 2X demultiplexing, the channels within a group of four cannot arbitrarily drive the others.	
	E3(7:0) to	E2(7:0), E1(7:0), E0(7:0) (TLA5204 only)
	A3(7:0) to	A2(7:0), D3(7:0), D2(7:0)
	A1(7:0) to	A0(7:0), D1(7:0), D0(7:0)
	C3(7:0) to	C2(7:0), C1(7:0), C0(7:0)
	CK3 to	CK2, Q3, Q2 (TLA5204 only)
	CK1 to	CK0, Q1, Q0

Table 7: TLA5200 clocking (cont.)

2X Demux clocking	
TLA5201, TLA5202	Unlike 2X demultiplexing, the channels within a group of four cannot arbitrarily drive the others.
	A1(7:0) to A0(7:0), D1(7:0), D0(7:0) TL:A5202 only
	C3(7:0) to C2(7:0), A3(7:0), A2(7:0)
Time between Demultiplex clock edges *(Typical)*	Same limitations as normal synchronous acquisition
Clocking state machine	
Pipeline delays	Each channel can be programmed with a pipeline delay of 0 through 7 active clock edges.

1 It is possible to use storage control and only store data when it has changed (transitional storage).

2 Applies to asynchronous clocking only. Setup and hold window specification applies to synchronous clocking only.

3 Any or all of the clock channels may be enabled. For an enabled clock channel, either the rising, falling, or both edges can be selected as the active clock edges. The clock channels are stored.

4 All qualifier channels are stored. For custom clocking there are an additional 4 qualifier channels on C2 3:0 regardless of channel width.

Table 8: TLA5200 trigger system

Characteristic	Description
Triggering Resources	
Word/Range recognizers	16 word recognizers. The word recognizers can be combined to form full width, double bounded, range recognizers. The following selections are available:
	16 word recognizers 0 range recognizers
	13 word recognizers 1 range recognizer
	10 word recognizers 2 range recognizers
	7 word recognizers 3 range recognizers
	4 word recognizers 4 range recognizers
Range recognizer channel order	From most-significant probe group to least-significant probe group: C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0 CK3 CK2 CK1 CK0
	Missing channels for instruments with fewer than 136 channels are omitted.
Glitch detector [1 2]	Channel groups can be enabled to detect glitches.
	Glitches are subject to pulse width variations of up to ±125 ps
Minimum detectable glitch pulse width *(Typical)*	1.25 ns (single channel with P6434 probe)
	1.0 ns (P6410, P6417, P6418, P6419 probe)
Setup and hold violation detector [1 3]	Any channel can be enabled to detect a setup or hold violation. The range is from 8.0 ns before the clock edge to 8.0 ns after the clock edge in 0.125 ns steps. The channel setup and hold violation size can be individually programmed.
	The range can be shifted towards the positive region by 0 ns, 4 ns, or 8 ns. With a 0 ns shift, the range is +8 ns to -8 ns; with a 4 ns shift, the range is +12 ns to -4 ns; with an 8 ns shift, the range is +16 ns to 0 ns. The sample point selection region is the same as the setup and hold window.
	Any setup value is subject to variation of up to the channel skew specification. Any hold value is subject to variation of up to the channel skew specification.

Table 8: TLA5200 trigger system (cont.)

Characteristic	Description
Transition detector [1]	16 transition detectors. Any channel group can be enabled or disabled to detect a rising transition, a falling transition, or both rising and falling transitions between the current valid data sample and the previous valid data sample.
Counter/Timers	2 counter/timers, 51 bits wide, can be clocked up to 500 MHz. Maximum count is 2^{51}-1. Maximum time is 4.5 X 10^6 seconds or 52 days. Counters and timers can be set, reset, or tested and have zero reset latency.
External Signal In [1]	A backplane input signal.
External Trigger In	A backplane input signal that causes both the main acquisition and the MagniVu acquisition to trigger if they are not already triggered.
Active trigger resources	16 maximum (excluding counter/timers) Word recognizers are traded off one-by-one as External Signal In, glitch detection, setup and hold detection, or transition detection resources are added.
Trigger States	16
✓ Trigger State sequence rate	Same rate as valid data samples received, 500 MHz maximum.
Trigger Machine Actions	
Main acquisition trigger	Triggers the main acquisition memory.
Main trigger position	Trigger position is programmable to any data sample (2 ns boundaries).
MagniVu™ acquisition trigger	Triggering of MagniV memory is controlled by the main acquisition trigger machine.
MagniVu™ trigger position	The MagniV trigger position is programmable within 2 ns boundaries and separate from the main acquisition memory trigger position.
Increment & decrement counter	Either of the two counter/timers used as counters can be increased or decreased.
Reloadable word recognizer	Loads the current acquired data sample into the reference value of the word recognizer via a trigger machine action. All data channels are loaded into their respective word recognizer reference register on a one-to-one manner.
Reloadable word recognizer latency	378 ns
Start/Stop timer	Either of the two counter/timers used as timers can be started or stopped.
Reset counter/timer	Either of the two counter/timers can be reset. When a counter/timer is used as a timer and is reset, the timer continues from the started or stopped state that it was in prior to the reset.
Signal out	A signal sent to the backplane to be used by other instruments.
Trigger out	A trigger out signal sent to the backplane to trigger other instruments.
Storage Control	
Global storage	Storage is allowed only when a specific condition is met. This condition can use any of the trigger machine resources except for the counter/timers. Storage commands defined in the current trigger state will override the global storage control. Global storage can be used to start the acquisition with storage initially turned on (default) or turned off.

Table 8: TLA5200 trigger system (cont.)

Characteristic	Description
By event	Storage can be turned on or off; only the current sample can be stored. The event storage control overrides any global storage commands.
Block storage	When enabled, 31 samples are stored before and after the valid sample. Not allowed when glitch storage or setup and hold violation is enabled.
Glitch violation storage	The acquisition memory can be enabled to store glitch violation information with each data sample when asynchronous clocking is used. The probe data storage size is reduced by one half (the other half holds the violation information). The fastest asynchronous clocking rate is reduced to 4 ns.
Setup and hold violation storage	The acquisition memory can be enabled to store setup and hold violation information with each data sample when synchronous clocking is used. The probe data storage size is reduced by one half (the other half holds the violation information). The maximum clock rate in this mode is 235 MHz.

1 Each use of External Signal In, glitch detector, setup and hold violation detector, or transition detector requires a trade-off of one word recognizer resource.

2 Any glitch is subject to pulse width variation of up to the channel-to-channel skew specification + 0.25 ns.

3 Any setup value is subject to variation of up to the channel skew specification. Any hold value is subject to variation of the channel skew specifications.

Table 9: TLA5200 MagniVu feature

Characteristic	Description
MagniVu memory depth	16,000 samples per channel
MagniVu sampling period	Data is asynchronously sampled and stored every 125 ps in a separate high resolution memory. The storage speed may be changed (by software) to 250 ps, 500 ps, or 1000 ps so that MagniVu memory covers more time at a lower resolution.

Table 10: TLA5200 Data Placement

Characteristic	Description
System time zero placement error *(Typical)*	±4 ns + backplane 10 MHz skew All stored data is referenced to this point.
Data correlation error *(Typical)*	±200 ps + system time zero placement error
Relative timestamp accuracy *(Typical)*	±100 ps + sample uncertainty + backplane 10 MHz clock jitter and tolerance This specification can be used to indicate the accuracy of a time measurement between samples. When measuring between samples, only the time difference between samples should be used to indicate accuracy. For example, if one sample has a timestamp of one hour and another sample has a timestamp of one hour and 10 ms, the 10 ms is the period of time used to determine the amount of error caused by the 10 MHz clock tolerance.
Timestamp counter and resolution	125 ps resolution 3.25 days duration

Table 11: TLA5200 Data handling

Characteristic	Description
Nonvolatile memory retention time *(Typical)*	Battery is integral to the NVRAM. Battery life is > 10 years.

Table 12: TLA5200B internal controller

Characteristic		Description
Operating system		Microsoft Windows
Microprocessor		Intel Celeron, 2.93 GHz
Main memory	Style	184 pin DDR2 SDRAM DIMM gold-plated
	Speed	266 MHz DDR2 PC2100
	Installed configuration	512 MB
	Maximum configuration	4 GB (four 1 GB DIMMs)
Cache memory		Level 2 (L2) Write-back cache
	Capacity	256 KB
	Style	Integrated
Real-time clock and CMOS setups NVRAM		Real-time clock/calendar. Standard and advanced PC CMOS setups. Battery life is typically > 3 years when the logic analyzer is not connected to line voltage. When connected to line voltage the life of the battery is extended. Lithium battery, CR2032
Hard disk drive		80 GB standard PC compatible IDE (Integrated Device Electronics) hard disk drive residing on a serial ATA interface. Continually subject to change due to the fast-moving PC component environment. Storage capacities valid at product introduction.
CD-DVD drive		Standard PC compatible IDE (Integrated Device Electronics) CD-RW/DVD-R drive residing on an EIDE interface. Continually subject to change due to the fast-moving PC component environment.
Floppy disk drive		Standard 3.5 inch 1.44 MB PC compatible high-density, double-sided floppy disk drive on the USB bus

Table 13: TLA5200 internal controller

Characteristic		Description
Operating system		Microsoft Windows
Microprocessor		Intel Celeron, 2 GHz
Main memory		PC2100 DDR SDRAM
	Style	184 pin DIMM, 2 Sockets
	Speed	100 MHz
	Installed configuration	512 MB loaded in one socket

Table 13: TLA5200 internal controller (cont.)

Characteristic	Description
Real-time clock and CMOS setups, plug & play NVRAM retention time	Battery life is typically > 3 years when the logic analyzer is not connected to line voltage. When connected to line voltage the life of the battery is extended. Lithium battery, CR2032
Hard disk drive	80 GB standard PC compatible IDE (Integrated Device Electronics) hard disk drive residing on an EIDE interface. Continually subject to change due to the fast-moving PC component environment. Storage capacities valid at product introduction.
CD-RW drive	Standard PC compatible IDE (Integrated Device Electronics) CD-RW drive residing on an EIDE interface. Continually subject to change due to the fast-moving PC component environment.
Floppy disk drive	Standard 3.5 inch 1.44 MB PC compatible high-density, double-sided floppy disk drive.

Table 14: TLA5200 display system

Characteristic		Description		
Display memory		8 MB SDRAM-onboard the ATI Mobility I video controller		
Display selection		Hardware sense of external SVGA monitor connected to the external primary display connector prior to the BIOS boot sequence enables the operation of that display output. The internal LCD display is enabled at all times. The internal LCD and the primary external displays operate at the same resolution (limited to 1024 X 768 on current TFT LCD) and display rates. Dynamic Display Configuration 1 (DDC1) support for the external SVGA monitor is provided.		
Display modes		Three displays can be driven independently, the LCD display and two external displays. The LCD display and one of the external displays are driven from the ATI RAGE Mobility M1 chip and are the primary displays; the two displays are independent. A third display is the second external display port driven from the motherboard (secondary display).		
External display drive		TwoVGa, SVGA, or XGA-compatible analog output ports. Display size selected via Windows		
	Primary display size (RAGE M1 chip)	*Resolution (pixels)*	*Colors*	*Refresh rates*
		1024 x 768, 1280 x 1024, or 1600 x 1200	256, 64 K, 16.8 M	60, 75, 85, 100
	Secondary display size (845GV chip)	*Resolution (pixels)*	*Colors*	*Refresh rates*
		640 x 480	256, 64 K, 16.8 M	60, 75, 85
		800 x 600	256, 64 K, 16.8 M	60, 75, 85
		1024 x 768	256, 64 K, 16.8 M	60, 75, 85
		1280 x 1024	256, 64 K, 16.8 M	60, 75, 85
		1600 x 1200	256, 64 K, 16.8 M	60, 75, 85
		1920 x 1440	256, 64K	60, 75

Table 14: TLA5200 display system (cont.)

Characteristic		Description
Internal Display	Classification	Thin Film Transistor (TFT) 10.4 inch active-matrix color LCD display; CCFL backlight; intensity controllable via software.
	Resolution	1024 x 768 pixels
	Color Scale	256K
	Refresh rate	60

Table 15: TLA5200 front-panel interface

Characteristic	Description
QWERTY	ASCII to support naming of files, traces, and keyboard equivalents of pointing device inputs for menus.
Special Function Knobs	Various functions

Table 16: TLA5200 rear-panel interface

Characteristic	Description
Parallel Interface Port (LPT)	25-pin sub-D Parallel Port Connector, Extended Parallel Port (EPP), or Enhanced Capabilities Port (ECP)
Serial Interface Port (COM 1)	9-pin male sub-D connector to support RS-232 serial port
Two USB Ports	Two USB 2.0 (Universal Serial Bus) compliant ports
SVGA Output Ports (SVGA OUT)	15-pin sub-D SVGA connectors (two each, one Primary, one Secondary)
Mouse Port	PS/2 compatible mouse port utilizing a mini DIN connector
Keyboard Port	PS/2 compatible keyboard port utilizing a mini DIN connector

Table 17: TLA5200 AC power source

Characteristic	Description
Source Voltage and Frequency	100 V_{RMS} to 240 V_{RMS} ±10%, 47 Hz to 63 Hz
Maximum Power Consumption	240 Watts line power maximum
Steady-State Input Current	4 A_{RMS} maximum
Inrush Surge Current	65 A maximum
Power Factor Correction	Yes
On/Standby Switch and Indicator	Front Panel On/Standby switch, with indicator. The power cord provides main power disconnect.

Table 18: TLA5200 cooling

Characteristic	Description
Cooling System	Forced air circulation (negative pressurization) utilizing two fans operating in parallel
Cooling Clearance	51 mm (2 in), sides and rear; unit should be operated on a flat, unobstructed surface

Table 19: TLA5200 mechanical characteristics

Characteristic	Description	
Overall Dimensions	(See Figure 1.)	
Weight	Includes empty accessory pouch and front cover	
	TLA5201	11.8 Kg (25 lb 15 oz)
	TLA5202	11.85 Kg (26 lb 2 oz)
	TLA5203	11.9 Kg (26 lb 4 oz)
	TLA5204	12 Kg (26 lb 7 oz)

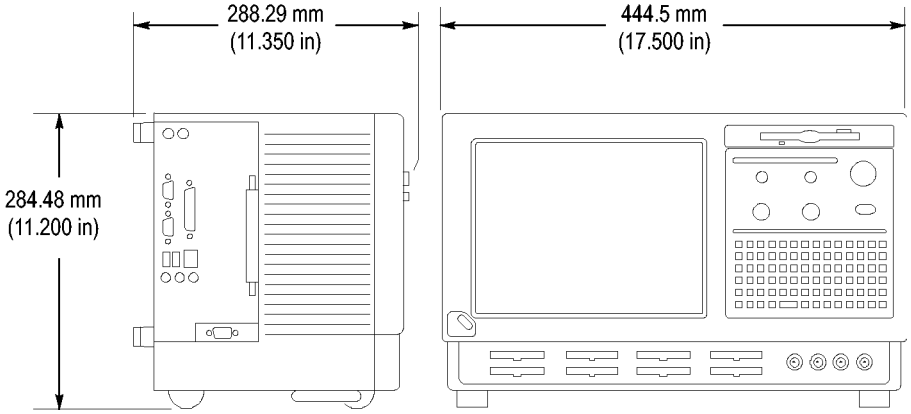


Figure 1: Dimensions of the TLA5200 series logic analyzer

External Oscilloscope (iView) Characteristics

The following table lists the characteristics for iView (Integrated View) and for the Tektronix logic analyzer when connected to an external oscilloscope. For detailed information on the individual specifications of the external oscilloscope, refer to the documentation that accompanies the oscilloscope.

Table 20: External oscilloscope (Integrated View or iView) characteristics

Characteristic	Description	
Supported Tektronix logic analyzer instruments	TLA5200 and TLA5200B series	
	TLA7012, TLA7016	
TLA application software version	V5.1SP1 or greater	
Minimum recommended TLA controller RAM [1]	256 MB	
Supported external oscilloscopes as of January, 2008 *(For the latest list of supported external oscilloscopes, visit our Web site at www.tektronix.com.)*	TDS1000, TDS2000 [2] [3], TDS1000B and TDS2000B Series [3] [4]	
	TDS3000 and TDS3000B Series (TDS3GM GPIB/RS-232 communication module required)	
	DPO4000 and MSO4000 Series [4]	
	TDS5000 and TDS5000B Series	
	TDS6000, TDS6000B, and TDS6000C Series	
	DPO7000 and DPO7000B Series	
	DPO70000 and DSA70000 series	
	TDS7000 and TDS7000B Series	
	CSA7000 and CSA7000B Series	
	TDS654C, TDS684C, TDS694C	
	TDS754C, TDS784C, TDS724D, TDS754D, TDS784D, TDS794D	
External oscilloscope software or firmware version number	*Product*	*Version*
	TDS684C, TDS694C	Any version
	TDS3000 series	Any version
	DPO4000 series	Any version
	TDS5000 series	Any version
	TDS6000 series	Any version
	DPO7000 series	Version 1.2 or greater
	TDS7000, CSA7000 series	
Maximum number of external oscilloscopes	One per Tektronix logic analyzer mainframe	
iView cable length [5]	6.56 ft (2 m)	

Table 20: External oscilloscope (Integrated View or iView) characteristics (cont.)

Characteristic	Description	
Time correlation uncertainty [6] (*Typical at system trigger)*	3 ns	Logic analyzer triggers external oscilloscope (2 ns + logic analyzer sample period + external oscilloscope sample period)
	5 ns	External oscilloscope triggers logic analyzer (4 ns + logic analyzer sample period + external oscilloscope sample period)

1 If RAM is less than 256 MB, the record length of the external oscilloscope may be limited to 1 M.

2 An GPIB extender is needed to connect the iView cable to the oscilloscope. One end of a standard GPIB cable can be used.

3 If you encounter possible alignment problems with the logic analyzer and oscilloscope waveform edges, refer to Aligning Logic Analyzer and Oscilloscope Waveform Edges. (See page 16, *Aligning Logic Analyzer and Oscilloscope Waveform Edges*.)

4 A GPIB to USB adapter (TEK-USB-488) is required to connect the iView cable to the oscilloscope.

5 When used with a TLA7016 mainframe and an external PC (such as TLA7PC1), the instruments must be physically located close together so that the iView cable can span both instruments. Removing the sleeving from the iView cable assembly increases the spacing distance available between the external PC and the TLA7016 mainframe.

6 Includes sampling uncertainty, typical jitter, slot-to-slot skew, and probe-to-probe variations to provide a typical number for the measurement.

Aligning Logic Analyzer and Oscilloscope Waveform Edges

The first time that you take an acquisition after changing the horizontal scale setting on TDS1000, TDS1000B, TDS2000, or TDS2000B series oscilloscopes, the logic analyzer and oscilloscope waveform edges may not be aligned within the listed specification. You can realign the waveform positions in the waveform window that contains the oscilloscope data (Menu bar > Data > Time Alignment). Make sure that the external oscilloscope is the data source and then adjust the time offset to align the waveforms. Use the following approximate offsets for various horizontal scale settings. (See Table 21.)

Table 21: TDS1000, TDS1000B, TDS2000, and TDS2000B Series oscilloscope waveform edge alignment

Horizontal scale	Time offset
100 ns	–5 ns
250 ns	–11 ns
500 ns	–18 ns
1 µs	–12 ns
2.5 µs	–50 ns
5 µs	–120 ns
10 µs	–250 ns
25 µs	–650 ns

Performance Verification Procedures

This chapter contains procedures for functional verification, certification, and performance verification procedures for the TLA5200 and TLA5200B series logic analyzer mainframes. Generally, you should perform these procedures once per year or following repairs that affect certification.

Summary Verification

Functional verification procedures verify the basic functionality of the instrument inputs, outputs, and basic instrument actions. These procedures include power-on diagnostics, extended diagnostics, and manual check procedures. These procedures can be used for incoming inspection purposes.

Performance verification procedures confirm that a product meets or exceeds the performance requirements for the published specifications documented in the *Specifications* chapter of this manual. The performance verification procedures certify the accuracy of an instrument and provide a traceability path to national standards.

As you complete the performance verification procedures, you can fill out a calibration data report to keep on file with your instrument. A blank copy of the calibration data report is provided with this manual. The calibration data report is intended to be copied and used to record the results of the calibration/certification procedures.

Certification

The system clock of the controller is checked for accuracy, and the input probe channels are checked for threshold accuracy and setup and hold accuracy. The instrument is certifiable if these parameters meet specifications. Complete the performance verification procedures and record the certifiable parameters in a copy of the Calibration Data Report at the end of this chapter.

Test Equipment

These procedures use external, traceable signal sources to directly test characteristics that are designated as checked ✓ in the *Specifications* chapter of this manual. Always warm up the equipment for 30 minutes before beginning the procedures.

Table 22: Test equipment

Item number and description		Minimum requirements	Example
1.	Logic analyzer	TLA5200 or TLA5200B series logic analyzer	TLA5201, TLA501B, TLA5202, TLA5202B, TLA5203, TLA5203B, TLA5204, TLA5204B
2.	Logic analyzer probes	General purpose Tektronix logic analyzer probes; one probe required for every 17 channels.	P6410, P6417, or P6418
3.	Frequency counter	Frequency accuracy: <0.0025% Frequency range: 1 kHz to 100 MHz	Agilent 33131A
4.	Digital timing generator [1]	>235 MHz, ± 0.1% accuracy DC output: 0–5 V, ± 0.1% accuracy	Tektronix DTG5274
5.	DC voltage source (see footnote)	0–5 V, ± 0.1% accuracy	Tektronix PS281
6.	Digital multimeter with probes [2]	6.5 digit display, 35 ppm, 1 year accuracy, 1000 readings per minute	Fluke 8845A/8846A
7.	Cable, precision 50 Ω coaxial	50 Ω, 36 in, male-to-male BNC connectors	Tektronix part number 012-0482-XX
8.	Setup and Hold test fixture	User-built (See page 30, *Test Fixtures*.)	
9.	Threshold Accuracy test fixture	User-built (See page 30, *Test Fixtures*.)	

[1] Some timing generators (for example, the Tektronix DTG5274) include an internal DC voltage source that can be used instead of a separate power source.

[2] Only needed to verify the output of the voltage source if the source does not meet specification. In this case, the DMM becomes the traceable instrument.

Functional Verification

The following table lists functional verification procedures for the benchtop and portable mainframes. If necessary, refer to the *TLA5200B Series Logic Analyzer Installation Manual* for installation instructions.

Table 23: Functional verification procedures

Instrument	Procedure
TLA5200 Series logic analyzers	Power-on and fan operation
	Power-up diagnostics
	Extended diagnostics
	CheckIt Utilities diagnostics

Power-on and Fan Operation

Complete the following steps to check the power-on and fan operation of the logic analyzer:

1. Power on the instrument and observe that the On/Standby switch illuminates.
2. Check that the fans spin without undue noise.
3. If there are no failures indicated, the power-on diagnostics pass when you power on the mainframe(s).

Extended Diagnostics

Do the following steps to run the extended diagnostics:

NOTE. *Running the extended diagnostics will invalidate any acquired data. If you want to save any of the acquired data, do so before running the extended diagnostics.*

Prerequisites Warm-up time: 30 minutes

Perform the following tests to complete the functional verification procedure:

1. If you have not already done so, power on the instrument and start the logic analyzer application if it did not start by itself.
2. Go to the System menu and select Calibration and Diagnostics.
3. Verify that all power-on diagnostics pass.
4. Click the Extended Diagnostics tab.
5. Select All Modules, All Tests, and then click the Run button on the property sheet.

   All tests that displayed an "Unknown" status will change to a Pass or Fail status depending on the outcome of the tests.
6. Scroll through the tests and verify that all tests pass.

CheckIt Utilities

CheckIt Utilities is a comprehensive software application used to check and verify the operation of the hardware in the instrument. To run the software, you must have either a keyboard, mouse, or other pointing device.

NOTE. *To check the DVD/CD drive, you must have a test disc installed before starting the CheckIt CD-ROM test. The disc needs to contain a file with a size between 5 MB and 15 MB.*

To run CheckIt Utilities, follow these instructions:

1. Quit the logic analyzer application.
2. Click the Windows Start button.
3. Select All Programs → CheckIt Utilities.
4. Run the tests. If necessary, refer to the CheckIt Utilities online help for information on running the software and the individual tests.

Performance Verification

This section contains procedures to verify that the instrument performs as warranted. Verify instrument performance whenever the accuracy or function of your instrument is in question.

Tests Performed

Do the following tests to verify the performance of the TLA5200 Series logic analyzers. (See Table 24.) You will need test equipment to complete the performance verification procedures. (See Table 22 on page 18.) If you substitute equipment, always choose instruments that meet or exceed the minimum requirements specified.

Also note that setup procedures for your equipment may differ from those described in the procedures, due to changes in the equipment or firmware. For example, output connectors might be BNC or SMA, and setup menus can differ between models.

Table 24: Parameters checked by verification procedures

Parameter	Verification method
System clock (CLK10) accuracy [1]	Verified by the 10 MHz system clock test
Threshold accuracy [1]	Verified by the threshold accuracy test. Certified by running the certification procedure.
Setup and hold window size (data and qualifiers)	Verified directly by setup and hold procedure.
Channel-to-channel skew	Verified indirectly by the setup and hold procedure
Internal sampling period	Verified indirectly by the 10 MHz system clock test
Minimum recognizable word (across all channels)	Verified indirectly by the setup and hold procedure and by the Internal Sampling Period
Maximum synchronous clock rate	Diagnostics verify the clock detection/sampling circuitry. Bandwidth is verified indirectly by the at-speed diagnostics, the setup and hold test, and the clock test.
Counters and timers	Verified by diagnostics
Trigger state sequence rate	Verified indirectly by at-speed diagnostics

[1] Certifiable parameter

Prerequisites

The logic analyzer, test fixture, and other related test equipment must be installed, connected, and operating for at least 30 minutes at an ambient temperature between +20 C and +30 C.

Checking the 10 MHz System Clock (CLK10)

The following procedure checks the accuracy of the 10 MHz system clock:

Equipment required	Frequency counter Precision BNC cable
Prerequisites	Warm-up time: 30 minutes

1. Verify that all of the prerequisites above are met for the procedure.
2. Connect the frequency counter to the External Signal Out BNC connector on the instrument.
3. Select System Configuration from the System menu.
4. In the System Configuration dialog box, select 10 MHz Clock from the list of routable signals in the External Signal Out selection box and click OK.
5. Verify that the output frequency at the External Signal Out connector is 10 MHz ±1 kHz. Record the measurement on a copy of the calibration data report and disconnect the frequency counter.
6. In the System Configuration dialog box, reset the External Signal Out signal to None.

Threshold Accuracy

This procedure verifies the threshold voltage accuracy of the logic analyzer.

Equipment required	Precision voltage reference or a DC signal generator and precision digital voltmeter Threshold Accuracy test fixture Logic analyzer probe
Prerequisites	Warm-up time: 30 minutes

Test Equipment Setup

Connect a P6410, P6417, or P6418 probe from the logic analyzer to the voltage source, using the Threshold Accuracy test fixture. If the voltage source does not have the required output accuracy, use a multimeter with the required accuracy to verify the voltage output levels specified in the procedure.

TLA5200 Setup

To set up the logic analyzer for this test, you must define the characteristics of the channel that you are testing, and then set the trigger parameters:

1. Open the Setup window, and in the Probe Channel table, delete all the groups. You will define new groups in the following steps.
2. In the Group column, enter a name for the probe group that you are testing ("Test" in the example).
   a. Define the probe channels for the group that you are testing.
   b. Set the clocking to Internal, 2 ns.
   c. Set Acquire to Normal.
   d. Set the Memory Depth to 128 K or less.

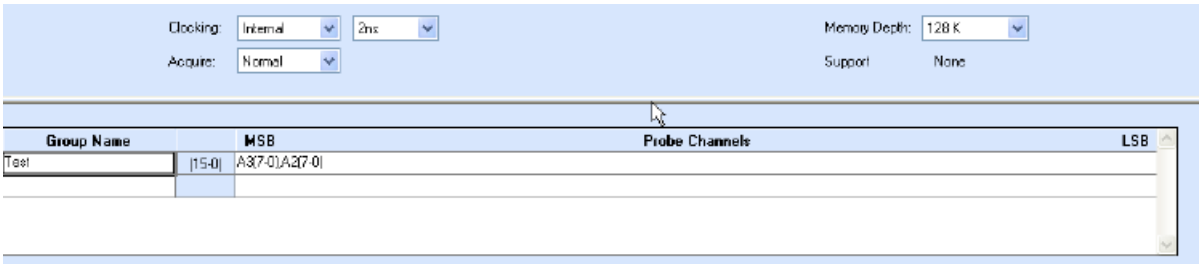


Figure 2: Defining group parameters

4. Go to the Trigger window and select the Power Trigger tab. Create a trigger program that triggers the logic analyzer when it doesn't see all highs or all lows:

   a. Click the If Then button.

   b. Set the channel definition to match the figure below.

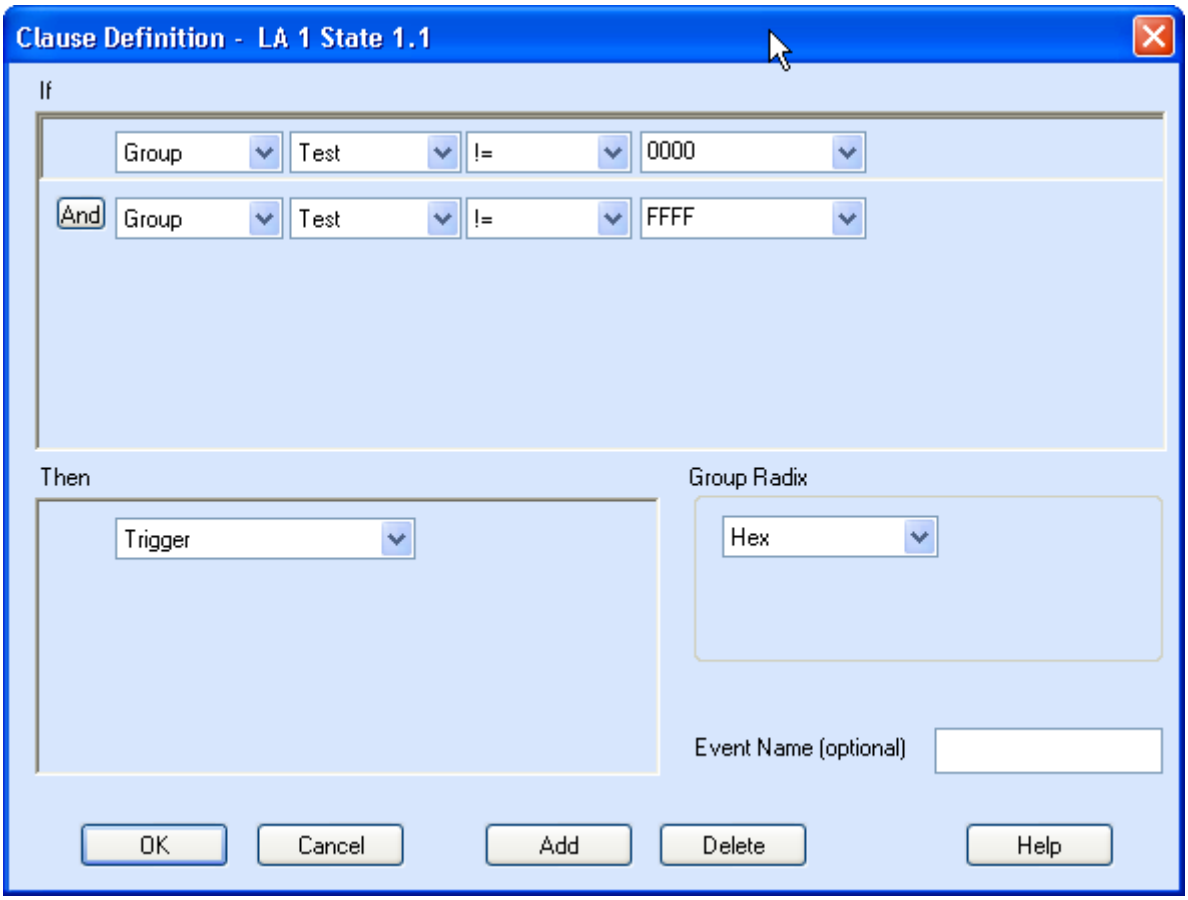


Figure 3: Setting trigger parameters

   c. Click OK.

Verification Procedure

Complete the following steps to complete this procedure. Record the results on the copy of the Calibration Data Sheet.

1. Go to the Setup window of the logic analyzer and set the probe threshold voltages to 4 V.
2. Set the voltage source to 3.88 V.
3. Start the logic analyzer and verify that it does not trigger.
4. Increase the voltage in 10 mV steps, waiting at least 3 seconds between steps to make sure that the logic analyzer continues to run without triggering. Continue until the logic analyzer triggers and then record the voltage.
5. Set the voltage source to 4.12 V.
6. Start the logic analyzer and verify that it does not trigger.
7. Decrease the voltage in 10 mV steps, waiting at least 3 seconds between steps to make sure that the logic analyzer continues to run without triggering. Continue until the logic analyzer triggers and then record the voltage.
8. Add the two voltage values and divide by two. Verify that the result is 4.00 V ±100 mV. Record the voltage on the Calibration Data Sheet.
9. Go to the Setup window and set the logic analyzer threshold voltages to –2.0 V.
10. Repeat steps 3 through 8 for –2.12 V and –1.88 V.
11. Repeat the procedure for each probe channel group that you want to verify.

Setup and Hold

This procedure verifies the setup and hold specifications of the logic analyzer.

Equipment required	Digital timing generator Precision BNC cable Setup and Hold test fixture
Prerequisites	Warm-up time: 30 minutes

Digital Timing Generator Setup

1. Verify that the digital timing generator (DTG) has been calibrated so that the channel-to-channel skew is minimized.
2. Set up the DTG so that a channel (CH1 for example), is set to be a clock pattern of alternating 1 and 0 (101010… binary) starting with 1 (rising edge).
3. Set the output frequency to 235MHz. (This may require you to set the DTG base clock to 470 MHz for this pattern to represent 235 MHz at the channel output.)
4. Set another channel of the DTG (CH2 for example) to a data pattern representing half the period of CH1 (for example 001100110011...binary, starting with 00).
5. Connect the setup and hold test fixtures to the DTG channels that you have set up. Connect 50 Ω SMA terminations to the test fixtures.
6. Connect the DTG channel that you set up as a clock to the appropriate TLA CK[x] input.
7. Connect the other DTG channel to two of the TLA data channels that you want to test.

   If you want to test other TLA data channels simultaneously and your DTG has additional outputs available, set up those DTG channels like the first data channel, and connect them to the other logic analyzer channels that you want to test. (You will need another test fixture for each additional channel pair.) Otherwise, repeat the procedure for each new pair of logic analyzer channels.
8. Set the termination to open on each DTG channel.
9. Set the DTG output voltage levels to 2.50V High and 0.0V Low, with no offset.

TLA5200 Setup

1. Start the TLA Application and open the Setup Window.
2. Click the DM button to default the module.
3. Set the following parameters:
   a. Clocking: External
   b. Acquire: Normal
   c. Acquisition Length: 1K or greater
   d. Click More… Select the positive edge of the clock line that you will be using to clock the data (CK[x] in the example).
4. Close the External Clocking dialog box.
5. While still in the Setup window, open the Probes dialog box and select the Thresholds tab.
6. Enter .62 and click Set All.

   With the 50 Ω external termination attached at the SMA fixture end, this sets the logic analyzer threshold voltage levels to one-half the resulting termination voltage, which should be about 620 mV (not 1.25 V).
7. Create a new group: right click in the Group Name column.
8. Select Add Group from the pop-up window. Rename the new group Test.
9. In the Probe Channels column, enter the names of the two adjacent data channels that will be used to connect to CH2 of the DTG.

Trigger Logic. To complete the setup, you must configure a trigger to occur whenever the two data lines are neither 00 nor 11 (binary). This will capture the condition when the two data signals are 01 or 10, as they transition to their common values. To set this up, do the following:

10. Open the LA Trigger window and select the Power Trigger tab. Set up three states as shown. (See Figure 4 on page 28.)

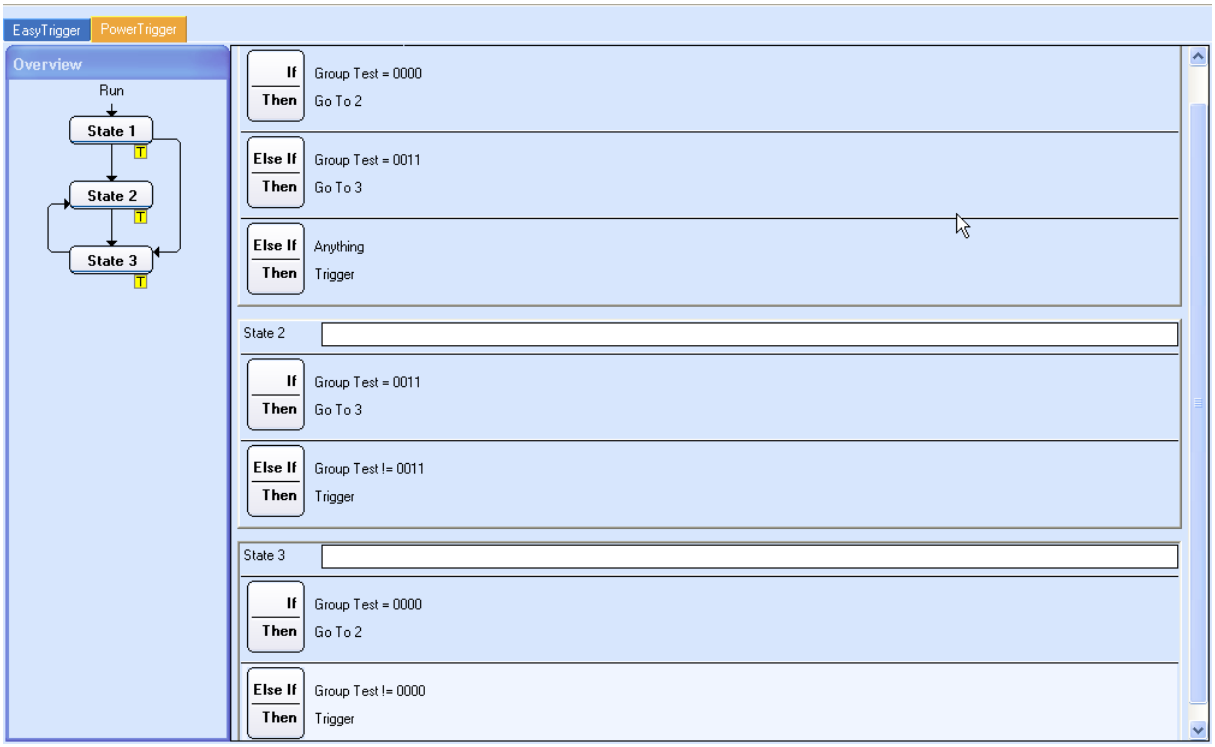


Figure 4: Set the trigger states

Verification Procedure

Complete the following steps to complete this procedure. Record the results on the Calibration Data Sheet.

1. Press the RUN button and wait a few seconds to verify that it doesn't trigger.
2. Increase the delay of the DTG clock channel (starting from 0.000 ns), until triggering begins to occur. Record this delay amount.

   Note that the logic analyzer might trigger because of a glitch when you make a delay change. If the data in the waveform window is correct (all data transitioning at the same time and at the correct frequency), then ignore this "false trigger" and start the logic analyzer again.

   As an alternative, you may want to run the logic analyzer in continuous loop mode if the DTG causes a false trigger on the logic analyzer each time you change the delay. Then observe if the data is correct in the waveform window and ignore any false triggers. Continue increasing the clock delay until the waveform window displays data that was not acquired correctly. Record this delay.
3. Add 1.00 ns to the delay value that you recorded in step 2 and increase the DTG clock delay to match this cumulative value. (For example, if you measured 0.85 ns, increase the delay to 1.85 ns.)
4. Press Run and wait a few seconds to verify that it doesn't trigger. This verifies that the setup and hold window is 1.00 ns or less, which is the guaranteed specification for a single channel. If you are testing more than one channel, you may need to add 1.50 ns to the value that you recorded in step 2 (1.5 ns is the typical specification for multiple channels).

   If you want to measure the actual setup and hold window size for your application, slowly decrease the clock delay in steps (waiting a few seconds between steps to verify that it doesn't trigger), until the logic analyzer triggers. Record this second value. The difference between this second value and the value that you measured in step 2 is the measured setup and hold window size.

Test Fixtures

This section includes information and procedures for building the test fixtures used in the performance verification tests.

Threshold Accuracy Test Fixture

Use this fixture to gain access to the logic analyzer probe pins. The fixture connects all ground pins together, and all signal pins together.

Equipment Required

You will need the following items to build the test fixture:

Item	Description	Example part number
Square-pin strip	0.100 x 0.100, 2 x 8 contacts (or two 1 x 8 contacts)	SAMTEC part number TSW-102-06-G-S
Wire	20 gauge	
Soldering iron and solder	50 W	

Build Procedure

Use the following procedure to build the test fixture.

1. Set the square-pin strip down and lay a wire across one row of pins on one side of the insulator as shown. Leave some extra wire at one end for connecting to a test lead. (See Figure 5.)
2. Solder the wire to each pin in the row.
3. Repeat for the other row of pins.

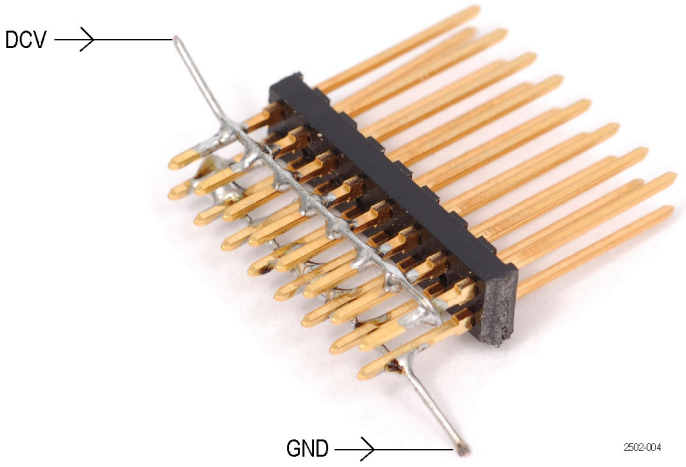


Figure 5: Threshold Accuracy test fixture

Setup and Hold Test Fixture

This fixture provides square-pin test points for logic analyzer probes when they are used to probe in-line SMA connections. Note that you need a minimum of two test fixtures to complete the procedure.

Equipment Required

You will need the following items to build the test fixture:

Item	Description	Example part number
SMA connector (two required for each fixture)	Female, PCB mount	SV Microwave part number 2985-6035, -6036, or -6037
Square-pin strip	0.100 x 0.100, 2 x 2 contacts (or two 1 x 2 contacts)	SAMTEC part number TSW-102-06-G-S
SMA termination	50 Ω, ≥2 GHz bandwidth	Johnson part number 142-0801-866
SMA adapter	Male-to-male	Johnson part number 142-0901-811
Soldering iron and solder	50 W	

Build Procedure

Use the following procedure to build the test fixture.

1. Arrange one SMA connector as shown. (See Figure 6.)
2. Align the square pins at a right angle to the connector.

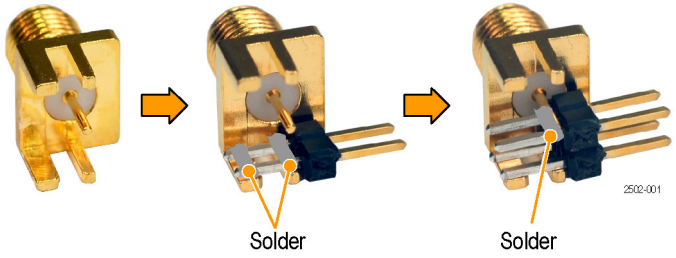


Figure 6: Solder square pins to the SMA connector

3. Solder one set of square pins to the SMA ground conductor.
4. Solder the other set of square pins to the SMA center conductor.

5. Align the second SMA connector to the first as shown and solder the center conductors of the connectors together. (See Figure 7.)

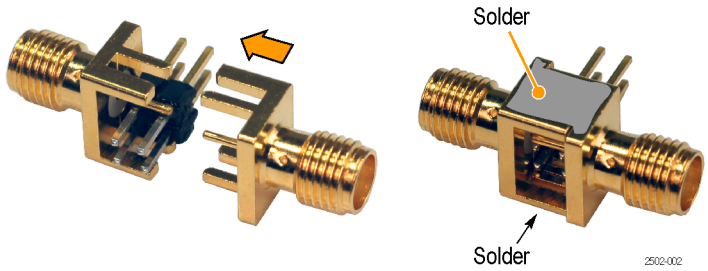


Figure 7: Solder the SMA connectors together

7. Solder the ground conductors of the SMA connectors together.
8. Attach the termination and coupler to the fixture.

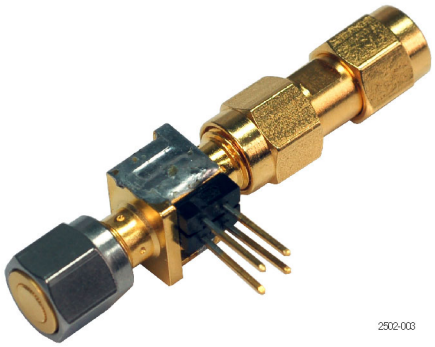


Figure 8: Completed fixture with termination and coupler

Calibration Data Report

Photocopy this table and use it to record the performance test results for your instrument.

TLA5200 Series

Instrument model number:
Serial number:
Certificate number:
Verification performed by:
Verification date:

Test Data

Characteristic	Specification	Tolerance	Incoming data	Outgoing data
Clock frequency	10 MHz	±1 kHz (9.9990 MHz-10.0010 MHz)		
Threshold accuracy	+4 V	±100 mV (3.900 V to 4.100 V)		
	-2 V	±100 mV (–1.900 V to –2.100 V)		
Setup and hold window:				
single channel	≤1.00 ns	none		
multiple channels	≤1.50 ns	none		